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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Attorney Docket No.	PHB 34,365 (7790/234)
Application Number	09/614,154
Filing Date	JULY 11, 2000
First Named Inventor	MARTIN J. EDWARDS
Group Art Unit	2677
Examiner	SHAPIRO, LEONID

ENCLOSURES *(check all that apply)*

☐ Amendment	☐ Assignment Papers *(for an Application)*	☐ Appeal Communication to Board of Appeals and Interferences
☐ After Final	☐ Drawings:	☒ Appeal Brief
☐ Affidavits/declaration(s)	☐ After Allowance Communication to Group	
	☐ Petition Routing Slip (PTO/SB/69) and Accompanying Petition	☐ Proprietary Information
☐ Status Letter	☐ To Convert a Provisional Application	☐ Post Card Receipt
☐ One-Month Petition for Extension of Time Request (duplic)	☐ Power of Attorney, Revocation Change of Correspondence Address	☐ Additional Enclosure(s) *(please identify below):*
☐ Express Abandonment Request	☐ Terminal Disclaimer	☐
☐ Information Disclosure Statement, PTO-1449, art	☐ Small Entity Statement	☐
☐ Certified Copy of Priority Document(s)	☐ Request of Refund	☐
☐ Response to Missing Parts/ Incomplete Application		

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account No. 50-1713. A duplicate copy of this sheet is enclosed.

☒ I hereby petition under 37 CFR § 1.136(a) for any extension of time required to ensure that this paper is timely filed. Please charge any associated fees which have not otherwise been paid to Deposit Account No. 50-1713. A duplicate copy of this sheet is enclosed.

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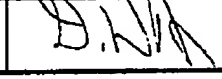
	Claims After Amendment		Highest No. Previously Paid For	Present Extra	Small Entity Rate	Small Entity Add'l Fee	or	Large Entity Rate	Large Entity Add'l Fee
Total		Minus		0	x $25=	0		x $50=	
Indep.		Minus		0	x $100=	0		x $200=	
First Presentation of Multiple Dep. Claim					+$180=	—		+ $360=	
					total add'l fee	$ 0		total add'l fee	$

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	DARRIN WESLEY HARRIS Registration No. 40,636 CARDINAL LAW GROUP 1603 Orrington Avenue, Suite 2000 Evanston, IL 60201		
Signature		Date	April 7, 2006

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PATENT
Case No. PHB 34,365
(7790/234)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re patent application of:

MARTIN J. EDWARDS

Serial No.: 09/614,154

Filed: JULY 11, 2000

For: ACTIVE MATRIX ARRAY DEVICES

Examiner: SHAPIRO, LEONID

Group Art Unit: 2673

APPEAL BRIEF

Mail Stop **Appeal Brief - Patents**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellant herewith respectfully presents a Brief on Appeal as follows:

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1. REAL PARTY IN INTEREST

The real party in interest is Koninklijke Philips Electronics N.V., a corporation of The Netherlands having an office and a place of business at Groenewoudseweg 1, Eindhoven, Netherlands 5621 BA. Koninklijke Philips Electronics N.V. is the ultimate parent of the assignee of record Philips Electronics North America Corporation, a Delaware corporation having an office and a place of business at 1251 Avenue of the Americas, New York, NY 10020-1104. Philips Electronics North America Corporation intends to further assign this application to Koninklijke Philips Electronics N.V.

2. RELATED APPEALS AND INTERFERENCES

Appellant and the undersigned attorney are not aware of any other appeals or interferences which will directly affect or be directly affected by or having a bearing on the Board's decision in the pending appeal.

3. STATUS OF CLAIMS

Claims 1-8 have been cancelled from the present application.

Claims 9-12 are currently pending in the present application, and are the claims on appeal. See, Claims Appendix.

Claim 13 has been allowed.

4. STATUS OF AMENDMENTS

Appellant filed an after final request for reconsideration under 37 C.F.R. §1.116 in response to a Final Office Action dated January 12, 2006. The request for reconsideration did not contain any claims amendments.

5. SUMMARY OF THE INVENTION

An active matrix array device of the present invention employs a substrate 25 (FIGS. 1, and 3-5), an array of individually addressable matrix elements 10 (FIG. 1) carried on substrate 25, a set of address conductors 16 (FIGS. 1-5) connected to elements 10 and carried on substrate 25, and an addressing circuit 35 (FIGS. 1, 2, 4 and 5) including a multiplexing circuit 31 (FIGS. 4 and 5) integrated on substrate 25 and connected to address conductors 16, and nine (9) signal processing circuits 42(1) - 42(9) integrated on substrate 25. See, *U.S. Patent Application Serial No. 09/614,154* at page 6, lines 5-31; page 7, lines 16-23; page 7, line 30 to page 8, line 3; page 8, line 20 to page 9, line 8; and page 11, line 3 to page 12, line 19.

As illustrated in FIG. 2, address conductors 16 are arranged in a series of groups with each group including successive address conductors with the first group being address conductors C1-C9 which are collectively controlled by a gate signal G1 via control circuit 37, the second group being address conductors C10-C18 which are collectively controlled by a gate signal G2 via control circuit 37, and so on and so on. Additionally, multiplexing circuit 31 couples sequentially each group of address conductors 16 to nine (9) signal bus lines V1-V9 with each address conductor in a group being coupled to a respective one of signal bus lines. Specifically, the first address conductor of each group (e.g., conductors C1 and C10) is connected to signal bus line V1. The second address conductor of each group (e.g., conductors C2 and C11) is connected to signal bus line V2. The third address conductor of each group (e.g.,

conductors C3 and C12) is connected to signal bus line V3. The fourth address conductor of each group (e.g., conductors C4 and C13) is connected to signal bus line V4. The fifth address conductor of each group (e.g., conductors C5 and C14) is connected to signal bus line V5. The sixth address conductor of each group (e.g., conductors C6 and C15) is connected to signal bus line V6. The seventh address conductor of each group (e.g., conductors C7 and C16) is connected to signal bus line V7. The eighth address conductor of each group (e.g., conductors C8 and C17) is connected to signal bus line V8. And, the ninth address conductor of each group (e.g., conductors C9 and C18) is connected to signal bus line V9. See, *U.S. Patent Application Serial No. 09/614,154* at page 8, line 20 to page 9, line 8.

As illustrated in FIGS. 3-5, signal processing circuits 42(1) - 42(9) are connected to signal bus lines V1-V9, respectively.

As illustrated in FIG. 3, signal processing circuits 42(1) - 42(9) are arranged juxtaposed (1-2-3-4-5-6-7-8-9) in a row in accordance with the state of the art prior to the present invention. This arrangement leads to problems with a display quality of the device in view of the fact that last address conductor C9 of the first group of address conductors 16 and first address conductor C10 of the second group of address conductors 16 are adjacent on substrate 25 as shown in FIG. 2, but signal processing circuit 42(9) and signal processing circuit 42(1) are not adjacent on substrate 25 as shown in FIG. 3. This problem is repeated for each last address conductor of an address conductor group

that is adjacent to the first address conductor of a succeeding address conductor group. See, *U.S. Patent Application Serial No. 09/614,154* at page 9, line 24 to page 11, line 14.

To solve this problem, as illustrated in FIG. 4, the present invention arranges signal processing circuits 42(1) - 42(9) in a row with a different physical order (i.e., 1-9-2-8-3-7-4-6-5) than the sequential order of video bus lines V1-V9 (i.e., 1-2-3-4-5-6-7-8-9) whereby signal processing circuit 42(1) and signal processing circuit 42(9) are adjacent on substrate 25. See, *U.S. Patent Application Serial No. 09/614,154* at page 11, line 23 to page 12, line 3.

In another solution to the prior art problem, as illustrated in FIG. 5, the present invention arranges signal processing circuits 42(1) - 42(9) in two rows with the first row (1-2-3-4) being offset from the second row (9-8-7-6) in a brick-like fashion whereby processing circuit 42(1) is adjacent both signal processing circuits 42(2) and 42(9) on substrate 25. See, *U.S. Patent Application Serial No. 09/614,154* at page 12, lines 6-19.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 9-12 stand finally rejected under 35 U.S.C. §112, ¶2 as being indefinite.

Claims 9 and 10 stand finally rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,166,715 to *Chang* et al. in view of U.S. Patent No. 5,021,774 to *Ohwada* et al.

Claim 12 stands finally rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,384,806 to *Chang* et al. in view of U.S. Patent No. 5,021,774 to *Ohwada* et al. and in further view of U.S. Patent No. 6,384,806 to *Matsueda* et al.

7. **ARGUMENT**

Indefiniteness Of Claims 9-12. The Appellant respectfully asserts that it is clear how the main objective of the present invention is achieved as shown in FIGS. 4 and 5 with the physical order of signal processing circuits 42(1)-42(9) being different than the prior art physical order shown in FIG. 3. Specifically, signal processing circuits 42(1) and 42(9) are adjacent on substrate 25 as shown in FIGS. 4 and 5, and signal processing circuits 42(1) and 42(9) are far apart on substrate 25 as shown in FIG. 3. Please note the teachings on page 4, lines 3-23 of the present application are directed to the drawbacks of FIG. 3, and the teachings on page 4, lines 23-28 are directed to overcoming the drawbacks of FIG. 3 as exemplary shown in FIGS. 4 and 5.

Furthermore, Examiner Shapiro's assertion that FIGS. 4 and 5 only show the physical ordering for only one group of address conductors as being the basis for this indefiniteness rejection is clearly unjustified in view of the fact that (1) the present invention clearly teaches multiple groups of address conductors in FIG. 2, and the fact that (2) FIGS. 4 and 5 are used to primarily to show the physical ordering of the signal processing circuits 42(1)-42(9) on substrate 25 in view of the multiple groups of address conductors shown in FIG. 2.

Withdrawal of the rejection of claims 9-12 under 35 U.S.C. §112, ¶2 as being indefinite is therefore respectfully requested.

Obviousness Standard. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

***Chang* and *Ohwada* In Combination**. Examiner Shapiro has correctly recognized *Chang*'s failure to teach or suggest the last limitation of independent claim 9. Specifically, as illustrated in FIGS. 3 and 4, *Chang* teaches signal processing circuit 245_1 to 245_{40} where signal processing circuit 245_1 is associated with the first address conductors PIX1, PIX41, PIX81, PIX121, PIX161, PIX201, PIX241, PIX281, PIX321, PIX361, PIX401, PIX441, PIX481, PIX521, PIX561 and PIX601 of groups 1-16, respectively, and where signal processing circuit 245_{40} is associated with the last address conductors PIX40, PIX80, PIX120, PIX160, PIX200, PIX240, PIX280, PIX320, PIX360, PIX400, PIX440, PIX480, PIX520, PIX560, PIX600 and PIX640 of groups 1-16, respectively. *Chang*'s fails to teach or suggest the last limitation of independent claim 9

by teaching signal processing circuit 245_1 and signal processing circuit 245_{40} are not adjacent as shown in FIG. 3.

Thus, *Ohwada* must teach or suggest the last limitation of independent claim 9 in order to establish a prima facie case of obviousness. However, Examiner Shapiro has erroneously interpreted *Ohwada* as teaching the last limitation of independent claim 9, because a proper reading of *Ohwada* reveals that *Ohwada* also fails to teach or suggest the last limitation of independent claim 9.

Specifically, the last limitation of independent claim 9 is each individual signal processing circuit being associated with a first address conductor of a first group and a last address conductor of a second group are adjacent on the substrate. This limitation is neither taught nor suggested by *Ohwada* by the disclosure of a multiplexor, a single group of address conductors and a single signal processing circuit. Specifically, as shown in FIGS. 1, 2 and 7, the multiplexor of *Ohwada* consists of a voltage generator 3, TFT elements 2, sampling lines 5, and sampling TFT elements 6 that operate to sample and hold video input signal V_V on capacitors 7 in a sequential manner during a beginning portion of a scanning period via signals ø and CP. During a final portion of the scanning period, all capacitors 7 are simultaneously discharged as a single group by the single group of address conductors via a voltage V_{ST}, where each address conductor consists of a TFT element 10, a buffer 11 and a signal electrode 12. As illustrated in FIG. 4, the video input signal V_V is a single signal coming from a single processing circuit. *Ohwada* clearly does not teach groups of address conductors and a plurality of

signal processing circuits, and thus fails to teach or suggest the last limitation of independent claim 9.

In summary, the last limitation of independent claim 9 is directed to FIGS. 4 and 5 of the present application, and therefore the combination of *Chang* in view of *Ohwada* unequivocally fails to teach the last limitation of independent claim 9. Additionally, *Chang* teaches away from the last limitation of independent claim 9 by teaching a sequential control by a shift register 230 of the switches A1, A2, B1 and B2 of each signal processing circuit 245_1 to 245_{40} that is simplified based on the sequential arrangement of signal processing circuit 245_1 to 245_{40} as shown in FIG. 3.

Obviousness Rejection of Claims 9 and 10. The Appellant respectfully traverses the obviousness rejection of claim 9, because neither *Chang* nor *Ohwada* disclose, teach or suggest "a plurality of signal processing circuits integrated on said substrate, each signal processing circuit being connected to a respective bus line, wherein a first signal processing circuit associated with a first address conductor of a first group of address conductors and a second signal processing circuit associated with a last address conductor of a second group of address conductors are adjacent on said substrate" as recited in independent claim 9.

Withdrawal of the rejection of independent claim 9 under 35 U.S.C. §103(a) as being unpatentable over *Chang* in view of *Ohwada* is therefore respectfully requested.

Claim 10 depends from independent claim 9. Therefore, dependent claim 10 includes all of the elements and limitations of independent claim 9. It is therefore respectfully submitted by the Applicant that dependent claim 10 is allowable over *Chang* in view of *Ohwada* for at least the same reason as set forth herein with respect to independent claim 9 being allowable over *Chang* in view of *Ohwada*. Withdrawal of the rejection of dependent claim 10 under 35 U.S.C. §103(a) being unpatentable over *Chang* in view of *Ohwada* is therefore respectfully requested.

Matsueda. The video bus lines V1-V9 (FIGS. 2-5) of the present invention are taught by *Matsueda* as a 6 bit signal bus line to multiplexing circuit 101 of *Matsueda* (FIG. 15), a 8 bit signal bus line to multiplexing circuit 101' of *Matsueda* (FIG. 16), and signal bus lines D1B-DuB and D1T-DuT to multiplexing circuits 101A and 101B, respectively, of *Matsueda* (FIG. 17). The teaching of the aforementioned bus lines arguably implies an existence of signal processing circuits for providing the 6 bit signal bus line to multiplexing circuit 101 of *Matsueda* (FIG. 15), an existence of signal processing circuits for providing the 8 bit signal bus line to multiplexing circuit 101' of *Matsueda* (FIG. 16), and an existence of signal processing circuits for providing signal bus lines D1B-DuB and D1T-DuT to multiplexing circuits 101A and 101B, respectively, of *Matsueda* (FIG. 17). However, if they exist, these implied signal processing circuits are not illustrated in FIGS. 15-17 of *Matsueda*, and more importantly, *Matsueda* fails to provide any teachings related to the physical order of

these implied signal processing circuits on the substrates for supporting circuits 101, 101', 101A and 101B, respectively. This is particular evidenced by the failure of *Matsueda* to state any display quality problem related to the physical order of these implied signal processing circuits on the substrates for supporting circuits 101, 101', 101A and 101B, respectively.

Thus, at best, the physical order of these implied signal processing circuits on the substrates for supporting circuits 101, 101', 101A and 101B, respectively, must be deemed to be no more than cumulative to the prior art illustrated in FIG. 3 of the present invention.

Obviousness Rejection of Claim 12. The Appellant respectfully traverses the obviousness rejection of dependent claim 12, because neither *Chang*, *Ohwada* nor *Matsueda* disclose, teach or suggest "wherein an order in which said signal processing circuits are arranged physically on said substrate is different than a physical order of said signal bus lines to which said signal processing circuit blocks are respectively connected" as recited in dependent claim 12.

Withdrawal of the rejection of dependent claim 12 under 35 U.S.C. §103(a) as being unpatentable over *Chang* in view of *Ohwada* and in further view of *Matsueda* is therefore respectfully requested.

Dated: **April 7, 2006**

Respectfully submitted,
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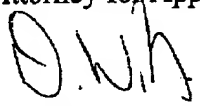

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CLAIMS APPENDIX

9. An active matrix array device, comprising:

a substrate;

an array of individually addressable matrix elements carried on said substrate;

a set of address conductors connected to said array of matrix elements and carried on said substrate, said set of address conductors being arranged in a series of groups with each group including successive address conductors; and

an addressing circuit including

a multiplexing circuit integrated on said substrate and connected to said set of address conductors, said multiplexing circuit including a plurality of signal bus lines, said multiplexing circuit being arranged to couple sequentially each group of said set of address conductors to said plurality of signal bus lines with each address conductor in a group being coupled to a respective one of said signal bus lines, and

a plurality of signal processing circuits integrated on said substrate, each signal processing circuit being connected to a respective bus line, wherein a first signal processing circuit associated with a first address conductor of a first group of address conductors and a second signal processing circuit associated with a last address conductor of a second group of address conductors are adjacent on said substrate.

10. The active matrix array device of claim 9, wherein said signal processing circuits are arranged in series in a line parallel to said multiplexing circuit.

11. The active matrix array device of claim 9, wherein a first subset of said signal processing circuits are arranged in a first row and a second subset of said signal processing circuits are arranged in a second row and offset from the first row in a brick-like fashion.

12. The active matrix array device of claim 9, wherein an order in which said signal processing circuits are arranged physically on said substrate is different than a physical order of said signal bus lines to which said signal processing circuit blocks are respectively connected.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.